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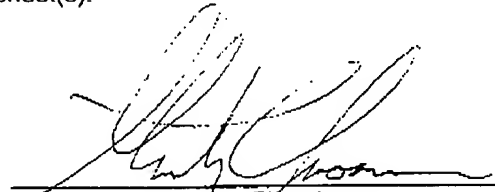
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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional)
		SCS-550-455
Application Number	Filed	
10/633,362	August 4, 2003	
First Named Inventor		
DIJKSTRA		
Art Unit	Examiner	
2181	J. Moll	
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p> <p>I am the</p> <p><input type="checkbox"/> Applicant/Inventor</p> <p><input type="checkbox"/> Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)</p> <p><input checked="" type="checkbox"/> Attorney or agent of record <u>27,393</u> (Reg. No.)</p> <p><input type="checkbox"/> Attorney or agent acting under 37CFR 1.34. Registration number if acting under 37 C.F.R. § 1.34 _____</p> <p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*</p> <p><input checked="" type="checkbox"/> *Total of 1 form/s are submitted.</p>		



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February 28, 2007
Date

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**STATEMENT OF ARGUMENTS IN SUPPORT OF
PRE-APPEAL BRIEF REQUEST FOR REVIEW**

The following listing of clear errors in the Examiner's rejection and his failure to identify essential elements necessary for a *prima facie* basis of rejection is responsive to the Final Rejection mailed September 29, 2006 (Paper No. 20060921) and the Advisory Action mailed February 20, 2007 (Paper No. 20070220).

Error #1. The Examiner fails to establish that the Applicant Admitted Prior Art (AAPA) discloses structures positively recited in independent apparatus claim 1 and independent method claim 22

(a) No disclosure of "address generation logic"

Independent claim 1 positively recites "address generation logic . . . for generating a shifted operand from one of said operands." In the outstanding Final Rejection, the Examiner alleges (on page 4) that this claimed structure is disclosed in "ADD unit 170." There is no evidence provided by the Examiner suggesting that ADD unit 170 can generate a "shifted operand" from one of the received operands. In fact, ADD unit 170 cannot possibly generate a shifted operand because it is not capable of generating a shifted operand.

The Examiner suggests use of a definition in the unsourced "Free On-line Dictionary of Computing," but that definition does not help the Examiner's case. There is no indication in that definition or anywhere else in the specification that multiplexer 130 (which is part of ADD unit 170) anticipates the features of Applicant's claim 1, i.e., the address generation logic for "generating a shifted operand from one of said operands." The multiplexer 130 in Figure 4 is capable of receiving a shifted operand as an input and merely outputs that same shifted operand, either directly or in inverted form. There is no disclosure identified by the Examiner which would lead one of

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ordinary skill in the art to believe that either multiplexer 130 or ADD unit 170 can generate a "shifted operand." The failure of the Examiner to provide any evidence to support his conclusion is evidence that the AAPA does not anticipate or render obvious the subject matter of independent claims 1 or 22.

(b) No disclosure of operand routing logic "for routing operands" as specified in claims 1 and 22

The Examiner suggests on page 5 of the Final Rejection that multiplexers 155 and 165 in Figure 5 are the equivalent to the claimed "operand routing logic." He also contends that shifter 160 in Figure 4 is a counterpart of the operand manipulation logic recited in claim 1.

However, a reading of Figure 4 (and the accompanying specification discussion of Figure 4) will show that, if the Examiner contends the shift circuitry 135 is a counterpart to the claimed operand manipulation logic and if the multiplexers 130 and 137 in Figure 4 are counterparts of the operand routing logic, the shift circuitry 135 being considered a counterpart of the address generation logic is completely inconsistent. Thus, the operand routing logic as set out in claim 1 is clearly missing from the AAPA.

The prior art arrangements in Figures 3A and 3B of the present specification disclose known arrangements which combine a shift and add operation. However, even if this previously known arrangement is considered to be a counterpart to the claimed "address generation logic," it could not be encompassed by claim 1 because there is no disclosed counterpart for the "operand routing logic."

As a result of the above, none of the prior art arrangements discussed with respect to Figures 1-5 in the present application anticipate the subject matter of independent claims 1 and 22. In order to establish a *prima facie* case, the Examiner must pick and choose different

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claimed elements from the different embodiments disclosed, i.e., the embodiment of Figures 3A and 3B, the embodiment of Figure 4, the embodiment of Figure 5. H

However, the burden is on the Examiner to identify a single disclosed embodiment which "anticipates" under §102 the subject matter of Applicant's claims. There is no single disclosed embodiment which contains all of the claimed elements and therefore there can be no *prima facie* case of anticipation. Additionally, because the burden is on the Examiner to establish a *prima facie* case, and since he has failed to meet this burden, there is simply no support for a rejection of independent claims 1 and 22 under 35 USC §102 or §103.

Error #2. The Examiner fails to provide any reason or motivation for combining different portions of the AAPA in the manner of Applicant's claims

Because, as noted above, Applicant's claimed combination of elements in claim 1 or method steps in claim 22 are not shown in any one embodiment (Figures 3A through Figure 5), the Examiner is not free to pick and chose elements from different embodiments and then combine them in the manner of the claims. It is incumbent upon the Examiner to establish some "reason" or "motivation" for picking and choosing elements from among the various prior art figures.

Thus, the Examiner's failure to meet the requirement of providing some "reason" or "motivation" for combining different portions of the AAPA prior art reference is simply not supported and the burden of proving the obviousness of a combination of elements has not been met.

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Error #3. The Examiner fails to properly construe the means-plus-function and step-plus-function claims

The Examiner summarily dismisses the Applicant's §112 (6th paragraph) claim construction argument by stating that "limitations from the specification are not read into the claims." This conclusion is clearly wrong in view of the statutory requirement of 35 USC §112 (6th paragraph) and the subsequent decisions by the Federal Circuit in *In re Donaldson* and its progeny.

The Examiner must demonstrate where the alleged prior art discloses positively recited claim limitations, such as "generating a shifted operand from one of said operands, and for adding together in dependence on said instruction, selected ones of said operands and said shifted operand to generate said address for subsequent processing by said pipeline stages." Where this exists in any prior art reference has not been shown by the Examiner.

This is the discussion as to the interrelationship between the operands received by the address generation logic and the operation of the generation logic, i.e., generating a shifted operand and for adding together one of the shifted operands with one of the regular operands as specified in the claim.

Applicant's claim states address generation logic "for receiving," "for generating" and "for adding." No structure for accomplishing these three functional interrelationships is set out anywhere else in the claim. Where a function is specified in a claim and no structure capable of performing that function is disclosed in the claim, the claim is to be construed as a means-plus-function claim, notwithstanding a presumption against means-plus-function status if the word "means" is not used ("the presumption here is overcome and the phrase 'colorant selection

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mechanism' should be construed as a means-plus-function limitation." *The Massachusetts Institute of Technology v. Abacus Software*, 80 USPQ2d 1225, 1231 (Fed. Cir. 2006)).

The Examiner's failure to properly analyze claim 1, to determine the limitations contained therein, i.e., structure which generates a shifted operand from one of the two received operands and for adding together selected ones of the operands and the shifted operand to generate an address, is simply a misunderstanding of how means-plus-function claims are to be properly construed. Without a proper understanding of the claim, it is of course impossible for the Examiner to demonstrate how or where Applicant's Admitted Prior Art contains any disclosure of the claimed structure.

SUMMARY

Properly claimed structures in claim 1 are not identified in the cited prior art – no disclosure anywhere in the prior art of the claimed "address generation logic" or the "operand routing logic. The Examiner provides no reason why one would combine elements taken from different embodiments of prior art, and certainly no reason why they would be combined in the manner of the independent claims. The Examiner misapplies Federal Circuit law regarding claim construction of "means-plus-function" claims and the lack of the word "means" is not dispositive that the claim is not to be construed in the manner of §112 (6th paragraph).

As a result of the above, there is simply no support for the rejection of Applicant's independent claims 1 and 22 or claims dependent thereon under 35 USC §102 or 103. Applicant respectfully requests that the Pre-Appeal Panel find that the application is allowed on the existing claims and prosecution on the merits should be closed.